In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-24. (Cancelled)

Claims 25. (Previously presented) A planar insulating layer with contact openings on a substrate having device areas comprised of:

a conducting layer having an anti-reflective coating on top surface and patterned to have open areas on said substrate;

said planar insulating layer on said patterned conducting layer having said contact openings of varying depths to said device areas, said contact openings formed using a single masking and etching step;

some of said contact openings extending down to and over an edge of said patterned conducting layer within said opening areas for forming low-resistance contacts to said edge of said patterned conducting layer, wherein at least two of said contact openings extending down to and over an edge of said patterned conducting layer within said opening areas are etched over said edge of said patterned conductive layer in said opening areas on opposite sides of said open areas to allow for more relaxed alignment tolerances.

Claim 26. (Cancelled)

Claim 27. (Original) The structure of claim 25, wherein a multiple of said contact opening are formed in series that is skewed to said edge of said patterned conducting layer on opposite side of said opening areas to allow for more relaxed alignment tolerance.

Claim 28. (Original) The structure of claim 25, wherein a multiple of said contact openings are etched in series along said edge of said patterned conducting layer in said open areas, and

wherein said contact openings are elongated normal to said edge of said patterned conducting layer in said opening areas to allow for more relaxed alignment tolerance.

Claim 29. (Original) The structure of claim 25, wherein said patterned conducting layer is the top electrode of a capacitor.

Claim 30. (Original) The structure of claim 25, wherein said anti-reflective coating is material selected form the group that includes silicon oxynitride, titanium nitride, and tantalum nitride, and is deposited to a thickness that minimizes the optical reflectivity during photoresist exposure.

Claim 31. (Previously presented) An integrated circuit, comprising:

a substrate;

a first device overlying a part of the substrate, wherein the first device having a plurality of contact regions formed in the substrate;

a first insulating layer overlying the substrate and the first devices;

a second device overlying a part of the first insulating layer, wherein the second device comprises a conductive layer having an overlying anti-reflective coating;

a second insulating layer overlying the second device and the first insulating layer;

at least one first opening through the first and second insulating layers, exposing a top surface of one of the contact regions; and

at least one second opening in the second insulating layer, exposing an edge of the conductive layer having an overlying anti-reflective coating of the second device.

Claim 32. (Previously presented) The integrated circuit of claim 31, wherein the at least one first opening has uniform depths to the second insulating layer.

Claim 33. (Previously presented) The integrated circuit of claim 31, wherein the at least one second opening has varying depths to the second insulating layer.

Claim 34. (Previously presented) The integrated circuit of claim 31, wherein the first device is a field effect transistor (FET) and the contact region is a source/drain region of the first device.

Claim 35. (Previously presented) The integrated circuit of claim 31, wherein the second device is a capacitor and the conductive layer is a top electrode of the second device.

Claim 36. (Previously presented) The integrated circuit of claim 31, wherein the second device is disposed over the first device.

Claim 37. (Previously presented) The integrated circuit of claim 36, further comprising a conductive contact in the first insulating layer between the first and second devices, electrically connecting thereof.

Claim 38. (Previously presented) The integrated circuit of claim 36, further comprising a plurality of first and second openings, wherein the first openings are substantially disposed over one of the contact regions of the first device and the second openings are substantially disposed over the edge of the conductive layer having an overlying anti-reflective coating of the second device to allow more relaxed alignment tolerances.

Claim 39. (Previously presented) An integrated circuit, comprising:

a substrate;

a first device and a second device overlying a part of the substrate, wherein the first device having a plurality of contact regions formed in the substrate and the second device comprises a conductive layer having an overlying anti-reflective coating;

a first insulating layer overlying the substrate and the first and second device;

at least one first opening through the first insulating layer, exposing a top surface of one of the contact regions; and

at least one second opening in the first insulating layer, exposing an edge of the conductive layer having an overlying anti-reflective coating of the second device.

Claim 40. (Previously presented) The integrated circuit of claim 39, wherein the at least one first opening has uniform depths to the first insulating layer.

Claim 41. (Previously presented) The integrated circuit of claim 39, wherein the at least one second opening has varying depths to the first insulating layer.

Claim 42. (Previously presented) The integrated circuit of claim 39, wherein the first device is a field effect transistor (FET) and the contact region is a source/drain region of the first device.

Claim 43. (Previously presented) The integrated circuit of claim 39, wherein the second device is a capacitor and the conductive layer is a top electrode of the second device.

Claim 44. (Previously presented) The integrated circuit of claim 39, wherein the second device is adjacent to the first device.

Claim 45. (Previously presented) The integrated circuit of claim 39, further comprising a plurality of first and second openings, wherein the first openings are substantially disposed over one of the contact regions of the first device and the second openings are substantially disposed over the edge of the conductive layer having an overlying anti-reflective coating of the second device to allow more relaxed alignment tolerance.

Claim 46. (New) An integrated circuit, comprising:

a substrate;

a first device overlying a first part of the substrate;

a second device overlying a second part of the substrate, wherein the second device comprises a conductive layer having an overlying anti-reflective coating;

at least one first contact connecting a top surface of the first device; and

at least one second contact connecting a sidewall of the conductive layer having the overlying anti-reflective coating of the second device.